

**SIDDHARTH INSTITUTE OF SCIENCE AND TECHNOLOGY: PUTTUR
(AUTONOMOUS)**

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QUESTION BANK (DESCRIPTIVE)

SUBJECT WITH CODE:	19EC0433-VLSI DESIGN	COURSE & BRANCH:	B.Tech - ECE
YEAR & SEM:	IV & I	REGULATION:	R19

UNIT –I

**INTRODUCTION AND BASIC ELECTRICAL PROPERTIES OF MOS AND Bi-CMOS
CIRCUITS**

1	a)	Summarize the evolution of microelectronics.	[L2][CO1]	[6 M]
	b)	Explain working of the NMOS transistor.	[L2][CO1]	[6 M]
2	a)	Illustrate about basic MOS transistors.	[L2][CO1]	[6 M]
	b)	Compare different modes in NMOS Transistor.	[L2][CO1]	[6 M]
3	a)	Define Metal Oxide Semiconductor VLSI Technology.	[L2][CO1]	[6 M]
	b)	List the advantages and disadvantages of IC.	[L1][CO1]	[6 M]
4	a)	Illustrate the steps involved in NMOS fabrication process with neat sketches.	[L2][CO2]	[6 M]
	b)	Discuss about body bias effect in the NMOS transistor.	[L2][CO1]	[6 M]
5		Explain the steps involved in P-Well CMOS fabrication process with neat sketches.	[L2][CO2]	[12M]
6	a)	Compare CMOS with bipolar technology in different aspects.	[L2][CO1]	[6 M]
	b)	State the different types of CMOS Process and illustrate the additional steps involved in Twin Tub Process.	[L2][CO2]	[6 M]
7	a)	Determine the relationship between I_{ds} & V_{ds} in non-saturated region.	[L3][CO2]	[6 M]
	b)	Explain in detail about Transconductance.	[L2][CO2]	[6 M]
8	a)	Derive the relationship between I_{ds} & V_{ds} in saturated region.	[L3][CO2]	[6 M]
	b)	Give the basic steps for IC fabrication.	[L2][CO2]	[6 M]
9	a)	Define output conductance and figure of merit	[L1][CO2]	[6 M]
	b)	Show the circuit diagram of BiCMOS inverter and explain its operations	[L4][CO2]	[6 M]
10	a)	What are the different forms of Pull Up Loads? which is the best choice for realization?	[L1][CO2]	[6 M]
	b)	Derive the expression for threshold voltage for MOS transistors.	[L3][CO2]	[6 M]

UNIT –II
VLSI CIRCUIT DESIGN PROCESS

1	a)	Explain the steps involved in VLSI Design flow.	[L2] [CO3]	[6M]
	b)	Construct the stick diagram of a 2-input CMOS NAND gate.	[L3] [CO3]	[6M]
2	a)	What are lambda-based design rules? Explain.	[L1] [CO3]	[6M]
	b)	Illustrate design rules for wires and MOS transistors.	[L2] [CO3]	[6M]
3	a)	Summarize 2μm based design rules with neat sketches.	[L2] [CO3]	[6M]
	b)	Draw the layout diagram of NMOS inverter circuit such that both input and output points are connected with Polysilicon layer.	[L4] [CO3]	[6M]
4	a)	Explain about Stick diagram with one example.	[L2] [CO3]	[6M]
	b)	Sketch the layout diagram for 2-input CMOS NAND gate.	[L3] [CO3]	[6M]
5	a)	Explain 2μm design rules for contacts and transistors.	[L2] [CO3]	[6M]
	b)	Sketch the layout diagram for CMOS inverter.	[L3] [CO3]	[6M]
6	a)	Construct stick diagram for $Y = (\overline{AB} + \overline{CD})$ in NMOS design style.	[L3] [CO3]	[6M]
	b)	Construct the layout diagram for 2-input CMOS NOR gate.	[L3] [CO3]	[6M]
7		Construct layout diagram for the logic equations in CMOS logic. (i) $Y = (\overline{A + B})\overline{C}$ (ii) $Z = (\overline{AB + CD})\overline{E}$	[L3] [CO3]	[12M]
8	a)	Illustrate λ-design rules for contact cuts.	[L2] [CO3]	[6M]
	b)	How a P-MOS transistor forms in lambda-based design rules? Explain.	[L1] [CO3]	[6M]
9	a)	Illustrate stick diagram of AND-OR-INVERTER in CMOS design Style.	[L2] [CO3]	[6M]
	b)	Explain about Implant and demarcation line in stick diagrams with neat sketches.	[L2] [CO3]	[6M]
10	a)	Construct the stick diagram for 2-input CMOS XOR gate.	[L3] [CO3]	[6M]
	b)	Explain different types of MOS layers used in VLSI circuits.	[L2] [CO1]	[6M]

UNIT –III
GATE LEVEL DESIGN & PHYSICAL DESIGN

1	a)	Sketch 2 x 1 mux using transmission gates.	[L3] [CO4]	[6M]
	b)	Explain the implementation of AOI using CMOS design style with neat sketches.	[L2] [CO4]	[6M]
2	a)	Draw the CMOS implementation of 4X1 mux using transmission gates?	[L1][CO3]	[6M]
	b)	Explain pseudo NMOS logic gate?	[L2][CO3]	[6M]
3	a)	What is switch logic? Explain with an example.	[L1] [CO4]	[6M]
	b)	Explain about pass transistors logic with an example.	[L2] [CO4]	[6M]
4	a)	What is pseudo NMOS logic? Explain with an example	[L1] [CO4]	[6M]
	b)	Construct 2-input NAND gate by using pseudo NMOS logic.	[L3] [CO4]	[6M]
5	a)	Explain dynamic CMOS logic circuit with an example.	[L2] [CO4]	[6M]
	b)	List the advantages & disadvantages of dynamic CMOS logic.	[L1] [CO4]	[6M]
6		Explain the following with an example.	[L2] [CO6]	[12M]
		(i) Domino CMOS logic. (ii) NOR A logic.		
7	a)	Explain the criteria for choice of layers.	[L2] [CO6]	[6M]
	b)	Explain about complex logic gates.	[L2] [CO4]	[6M]
8	a)	What is the necessity of floor planning concept in VLSI circuits? Discuss with suitable example.	[L2] [CO5]	[6M]
	b)	Explain the following terms: (i) Placement (ii) Routing	[L2] [CO5]	[6M]
9	a)	What are the design methods used in physical design cycle? Explain each term with suitable diagrams.	[L1] [CO4]	[6M]
	b)	What is routing? Explain about different routing techniques?	[L2] [CO3]	[6M]
10	a)	Discuss about the Power Estimation in CMOS circuit.	[L2] [CO5]	[6M]
	b)	Explain about Power delay estimation in VLSI circuits.	[L2] [CO5]	[6M]

UNIT –IV
SUBSYSTEM DESIGN

1	a)	Define the Counters in the digital circuit. Design 4-bit Asynchronous counter.	[L1] [CO4]	[6M]
	b)	Define Parity generator logic circuits. Design 4-bit Parity generator using EX-OR gate.	[L3] [CO4]	[6M]
2	a)	Explain different adder designs in sub circuit design with neat sketches.	[L2] [CO4]	[6M]
	b)	Differentiate Comparator and Magnitude Comparator with example.	[L4] [CO4]	[6M]
3	a)	What is shifter? List the types of shift registers and explain.	[L1] [CO4]	[6M]
	b)	Explain about 6 transistor Static memory cell.	[L2] [CO4]	[6M]
4		Explain the following logic circuit. (i) Parity Generator (ii) Comparator.	[L2] [CO4]	[12M]
5		Design an Arithmetic and Logic Unit circuit with four functions using multiplexers and explain its operation.	[L3] [CO4]	[12M]
6	a)	Compare different types of memory elements.	[L4] [CO4]	[6M]
	b)	Develop the 4x4 array multiplier.	[L3] [CO4]	[6M]
7	a)	Explain the working of Zero/one detector implemented with adder circuit.	[L2] [CO4]	[6M]
	b)	List the advantages and applications of Zero/one detector.	[L1] [CO4]	[6M]
8		Summarize the following. (i) Unsigned magnitude comparator. (ii) Asynchronous Counters.	[L2] [CO4]	[12M]
9	a)	Construct and explain the circuit diagram of 3-bit LFSR with example.	[L3] [CO4]	[6M]
	b)	Construct and explain the Johnson counter.	[L3] [CO4]	[6M]
10	a)	Construct and explain the circuit diagram of 4-bit Ripple Carry Adder.	[L3] [CO4]	[4M]
	b)	Construct and explain the ripple counter.	[L3] [CO4]	[4M]
	c)	Explain about 4 transistor Dynamic memory cell.	[L2] [CO4]	[4M]

UNIT –V
SEMICONDUCTOR INTEGRATED CIRCUIT DESIGN AND CMOS TESTING

1	a)	Compare PROM, PAL, and PLA with an example.	[L2] [CO6]	[6M]
	b)	Design the PAL Structure for the Boolean function $f_1(a,b,c,d)=ab+bc$ & $f_2(a,b,c,d)=ab+cd$.	[L3] [CO6]	[6M]
2	a)	Illustrate the architecture of FPGA with neat sketch.	[L2] [CO6]	[6M]
	b)	Discuss about the merits of FPGA over other PLD architectures.	[L2] [CO5]	[6M]
3	a)	Describe about CPLD structure in detail and explain each block.	[L1] [CO5]	[6M]
	b)	Generalize the design approach for VLSI system design.	[L2] [CO6]	[6M]
4		Design the following functions in PLA structure.	[L3] [CO5]	[12M]
		(i) $Y1=A'B'C'+ABC+A'B+ABC'$		
		(ii) $Y2=ABC+A'B'C+AC$		
		(iii) $Y3=A'BC'+AB'C+B'C'$		
5	a)	Explain in detail about standard cell design with suitable diagrams.	[L2] [CO6]	[6M]
	b)	Give examples of various fault models available for VLSI testing?	[L2] [CO6]	[6M]
6	a)	What is the need for testing? Explain about Fault simulation.	[L1] [CO6]	[6M]
	b)	Give a logic circuit example in which stuck-at-1 fault and stuck-at-0 fault are indistinguishable.	[L2] [CO6]	[6M]
7	a)	What is FPGA. Draw and explain basic structure of FPGA.	[L2] [CO5]	[6M]
	b)	Discuss about the Fault coverage and how to find it?	[L1] [CO6]	[6M]
8		Explain Chip Level Test techniques and its methodology.	[L2] [CO6]	[12M]
9	a)	What is testing? Explain any three test principles.	[L1] [CO6]	[6M]
	b)	What is controllability and observability? Give examples to explain it.	[L2] [CO6]	[6M]
10		What is BILBO? Draw the logic diagram of BILBO & explain its operation in different modes?	[L1 & L2] [CO6]	[12M]

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